ABSTRACT

Techniques for estimating a body voltage of one or more transistors which form digital partially depleted silicon-on-insulator circuit, and for using estimated voltages to analyze electrical properties of the circuit, are disclosed. In one technique, device models are obtained and abstracted to generate simplified electrical descriptions of the transistors. The circuit topology is checked to generate sets of accessible states for the transistors that are indicative of whether a connection between a source or a drain of a transistor and either a power supply or ground exists. Next, sets of reference state body voltage minima and reference state body voltage maxima are determined for each of the transistors based on corresponding simplified electrical descriptions and corresponding sets of accessible states. Finally, a target state body voltage minima and a target state body voltage maxima are ascertained, one for each transistor, based on the determined sets of reference state body voltage minima and reference state body voltage maxima.